IN THE CLAIMS

1 (Original). A power supply circuit comprising:

a switch state controller for producing a frequency modulated pulse train, a frequency of the pulse train controlled by a feedback signal coupled from an output characteristic of the power supply circuit, the switch state controller coupled to one of an input or internal node of the power supply circuit for controlling the on time of each pulse in the pulse train; and

a plurality of cascaded converter stages coupled between the input and the output, each of the cascaded converter stages having all switch control coupled to the switch state controller, whereby each of the plurality of converter stages is switched by the pulse train.

2 (Original). The power supply circuit of Claim 1, wherein the switch control of the converter stages comprises a single switch for controlling all of the converter stages.

3 (Original). The power supply circuit of Claim 1, wherein the input is a rectified AC voltage, the on-time is varied inversely with the RMS magnitude of the rectified AC voltage, and the first cascaded converter is one of a flyback type or boost type resulting in power factor corrected, low total harmonic distortion operation for a non-changing output.

4 (Original). The power supply circuit of Claim 1, wherein the switch state controller comprises a voltage-to-frequency converter for producing a pulse train of controlled period in conformity with a feedback signal.

5 (Original). The power supply circuit of Claim 1, further comprising a feedback circuit coupled to the switch state controller for controlling a frequency of the pulse train in conformity with an output characteristic of the power supply output.

6 (Original). The power supply circuit of Claim 5, wherein the feedback circuit comprises:

differential inputs wherein each terminal of the differential inputs is coupled to a separate transconductor; and

a current sensing element coupled to the differential inputs; and

the transconductors and the current sensing element allowing selection of arbitrary voltage across the current sensing element and choice of polarity.

7 (Original). The power supply circuit of Claim 6, wherein the feedback circuit further comprises a pair of integrators, wherein each integrator is coupled to one of the transconductors and the integrators being periodically reset.

8 (Original). The power supply circuit of Claim 7, wherein the feedback circuit further comprises a comparison circuit to determine which of the integrators is of greater peak amplitude at an end of an integration time and before being periodically reset.

9 (Original). The power supply circuit of Claim 8, wherein saturation of at least one of the integrators will result in an increase in a voltage to frequency control register voltage to allow startup.

10 (Original). The power supply circuit of Claim 8, further comprising a charge pump coupled to the output of the comparison circuit to control the pulse train period.

11 (Original). The power supply circuit of Claim 5, wherein the feedback circuit is adjusted with temperature.

12 (Original). The power supply circuit of Claim 6, wherein the feedback circuit further comprises a separate control input coupled to the differential input allowing adjustment of feedback in conformance with the control input.

13 (Original). The power supply circuit of Claim 12, wherein the control input is selected from a group consisting of: a PWM input signal, a voltage signal, a peak detected phase control signal, a voltage signal derived from an edge of a phase control signal, or a control signal derived from a LED brightness detector.

14 (Original). The power supply circuit of Claim 12, wherein the control input is a control input signal derived from a LED brightness detector.

15 (Cancelled).

16 (Original). The power supply circuit of Claim 1, wherein the switch state controller further comprises a voltage-to-frequency converter for producing the pulse train period in conformity with an output of the feedback circuit, and wherein an output of the comparator determines charging and discharging of a capacitor at the input of voltage-to-frequency converter.

17 (Original). The power supply circuit of Claim 16, wherein discharging of the capacitor produces a soft start of the power supply circuit by setting the period to a maximum length.

18 (Original). The power supply circuit of Claim 16, wherein the switch state controller further comprises:

integrator circuits which are reset in conformance with the period or group of periods;

a comparison circuit which compares outputs of the integrator circuits;

a charge pump circuit which controls the voltage on the capacitor coupled to the voltage to frequency converter each period in conformance with the comparison circuit;

the integrator circuits accepting feedback and causing the period to be adjusted in conformance with the feedback.

19 (Original). The power supply circuit of Claim 8, wherein the comparator further comprises a deadband for controlling ripple at the power supply output.

20 (Original). The power supply circuit of Claim 1, further comprising means for determining a control voltage of a voltage-to-frequency converter has exceeded a threshold, whereby a no-load condition is detected, and wherein the switch state controller disables the pulse width modulated output during the no-load condition.

21 (Original). The power supply circuit of Claim 18, wherein gating of the charge pump is suppressed in conformity with a control signal, causing the voltage to frequency converter to maintain constant period during a suppression time.

22 (Cancelled).

23 (Currently Amended). ~~An integrated circuit containing a switch state controller~~ A power supply circuit in accordance with Claim 1, wherein the switch state controller is used for producing a pulse train, a frequency of the pulse train controlled by a feedback signal coupled from an output characteristic of the power supply circuit to the switch state controller, the switch state controller further coupled to one of an input or internal node of a power supply circuit for controlling the on time of each pulse in the pulse train.

24 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~An integrated circuit of Claim 23,~~ wherein the feedback circuit is coupled to a frequency control input, the feedback circuit used for receiving a signal proportional to an output characteristic of the power supply circuit, for controlling the frequency in conformity with the output characteristic.

25 (Currently Amended). A power supply circuit in accordance with Claim 23 further comprising: ~~The integrated circuit of Claim 23, wherein the integrated circuit further comprises:~~

a gate terminal coupled to an output of the switch state controller for coupling to the control input of an external switch;

an input terminal for connecting to the power supply input;

a return terminal for receiving a return signal associated with the power supply input; and

a feedback terminal for receiving the output characteristic proportional signal.

26 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23,~~ wherein the feedback terminal comprises a pair of feedback terminals for receiving a differential voltage proportional to the output characteristic.

27 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23,~~ further comprising an internal high-voltage regulator coupled to the power supply input for providing an internal power supply to internal circuits.

28 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23,~~ further comprising an external terminal coupled to an internal high-voltage regulator for coupling to a capacitor external to the integrated circuit, whereby the internal power supply voltage can be filtered without filtering the power supply input and whereby the internal power supply voltage can be maintained at a sufficient voltage level for operation of the internal circuits.

29 (Cancelled).

30 (Original). The power supply circuit of Claim 1 wherein the power supply is mounted in close proximity to an LED load.

31 (Original). The power supply circuit of 30 wherein the power supply and LED load share a common heatsink.

32 (Original). The power supply circuit of 1 wherein all components have a life rating in excess of 10,000 hours at temperatures in excess of 90C.

33 (Original). The power supply circuit of Claim 1 wherein the power supply is mounted in close proximity to a display for backlighting.

34 (Original). The power supply of Claim 1 wherein the power supply is mounted in close proximity to one of an automotive headlight, tail light, indicator, center mount light, dome light, cluster backlight or reading light.

35 (Original). The power supply of Claim 1 wherein the power supply is configured as one of a retrofit to a MR16 lamp housing; a retrofit to a PAR38 lamp housing; or a retrofit to a miniature base lamps.

36 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23~~ further comprising an internal high-voltage regulator coupled to the rectified AC input voltage for providing an internal power supply to internal circuits.

37 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23,~~ further comprising an external terminal coupled to an internal high-voltage regulator for coupling to a capacitor element external to the integrated circuit.

38 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23,~~ further comprising a circuit which allows the integrated circuit to remain powered even when the high voltage input falls below the minimum voltage required by the integrated circuit by storing power in a capacitor coupled to a unidirectional high voltage regulator on the integrated circuit.

39 (Cancelled).

40 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23,~~ further comprising:

an undervoltage lockout circuit;

a shunt element for programming turn on/turn off voltage coupled to the integrated circuit; and

a sample and hold coupled to a VON pin.

41 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23,~~ further comprising:

an undervoltage lockout circuit;

a shunt element for programming turn on/turn off voltage coupled to the integrated circuit; and

one of na RMS filter or averaging circuit coupled to a VON pin.

42 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23~~ further comprising a linear transistor with high voltage terminal coupled to a DC voltage source.

43 (Currently Amended). A power supply circuit in accordance with Claim 23, ~~The integrated circuit of Claim 23~~ further comprising a protection circuit wherein the protection circuit comprises a clamp coupled to a pin and further coupled to a circuit which controls the on time such that a maximum on time is created when the clamp is active.

44 (Currently Amended). A power supply circuit in accordance with Claim 43, ~~The integrated circuit of Claim 43,~~ wherein the clamp comprises:

a resistor divider coupled from a DC input voltage to the VON pin; and

a diode coupled from a VDD pin to a resistor divider.

45 (Cancelled).

46. A power supply circuit in accordance with Claim 23, further comprising: ~~A power factor correction device comprising:~~

~~an integrated circuit containing a switch state controller wherein the switch state controller is used for producing a pulse train, a frequency of the pulse train controlled by a feedback signal coupled from an output characteristic of the power supply circuit, the switch state controller coupled to one of an input or internal node of a power supply circuit for controlling the on time of each pulse in the pulse train;~~

a resistor divider coupled to a rectified AC voltage source and to a VON pin; and

a filter coupled to the resistor divider to produce a filtered DC voltage at VON proportional to the RMS value of the rectified AC input voltage.

47 (Cancelled).

48 (Cancelled).